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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,122	12/29/2000	Shyh-An Chi	JCLA6705	8732

7590 11/25/2003

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EXAMINER	
O'BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	6

DATE MAILED: 11/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,122	CHI ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/29/00,3/12/01,5/12/01,9/14/01,2/24/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-14 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Miscellaneous Letter as received on 3/12/2001, Priority Papers as received on 5/12/2001, Change of Address as received on 9/14/2001, and Change of Address as received on 2/24/2003.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;

(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Claim Objections

5. Claim 6 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. The parent claim of claim 6 recites the limitation "a comparator, to receive the result signal and the predicted address and to output a comparison signal", while claim 6 recites the limitation "the comparison signal is generated after performing a comparison operation upon the result signal and the predicted address". Because a "comparator" inherently compares its inputs and outputs the result of the comparison, these limitations encompass the same scope. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

6. Claims 1, 5, and 9-12 are objected to because of the following informalities:

a. Regarding claim 1, as well as similar situations in claims 5, 9, and 12, the limitation "memory data access structure suitable for use in a processor" is recited. This claims a purported merit of the invention and thus should not be included in the claim language. Please remove this limitation from the claims mentioned, or simply change the limitation to read "memory data access structure in a processor."

b. Regarding claim 9, the claim recites the limitation "output to the cache memory", which has not antecedent basis. Please change the claim to either read "output to a cache memory", or to define the cache memory in the prior steps of the method as claimed.

c. Regarding claim 10, the claim recites the limitation "control" which has no antecedent basis. Please change the claim language to read "control signal", which will provide the claim with the correct antecedent basis with respect to its parent claim.

d. Regarding claim 11, it is unclear whether the claim language intends the method step to output the three signals claimed (result signal, address of instruction executed currently, signal with a certain value) at the same time when selected, or whether the method step selects between those signals. Furthermore, it is unclear from the claim language whether the limitation "address of the instruction executed currently plus a signal with a certain value" comprises an addition operation whose result is output, or two separate signals. Please correct the claim language to more distinctly point out the limitations of this claim.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. Claims 1, 5, 9 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These claims recite the limitation "fetching a fetch

instruction", or a derivative of it. It is unclear whether the "fetch instruction" comprises an instruction that has been fetched from a memory location, or whether the instruction performs a fetch operation, such as a load instruction. Please correct these claims to more distinctly point out and define the invention.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Potash, U.S. Patent No. 4,435,756, in further view of Patterson and Hennessy, *Computer Organization & Design*, 2nd Ed., 1998.

11. Regarding claim 1, Potash has taught a memory data access structure suitable for use in a processor, comprising:

a. A memory (M of Fig.1), to store and output an instruction according to an address signal (see Col.1 lines 16, 19-20 and Col.6 lines 33-36).

b. A pipeline processor (see Col.1 lines 10-18) for executing a plurality of processor instructions, the pipeline processor including an execution unit ("EX" of Fig.1) to perform an execution operation on the instruction input from a previous stage (see Col.1 lines 30-37), and to output a result signal (see Col.1 lines 25-28, 47-48) and

a control signal (64A of Fig.7), wherein the control signal is output to the memory (see Col.7 lines 35-52 and Col.8 lines 6-12), wherein

i. When the instruction executed by the execution unit is a branch instruction, the result signal is a target address, wherein the target address is selected to be an address signal output to the memory, wherein the memory fetches a next instruction to be executed according to the address signal (see Col.2 lines 35-46).

12. Potash has not explicitly taught a cache memory for storing and outputting an instruction according to an address signal, nor fetching the fetch instruction from an external memory according to a control signal if the instruction is not in the cache memory.

13. However, Patterson has taught the use of a memory hierarchy in modern microprocessors, consisting of multiple levels of memory of varying size and speed in order to create the appearance of a larger, faster memory space, while keeping costs minimized versus having a single large memory (see p.541-2). Furthermore, the general configuration of this hierarchy consists of a cache between the main memory and the processor (see p.545), which operates in a manner such that when a fetch of data at an address results in a cache miss, the data is instead brought from memory into the cache and processor (see p.545, 550). Therefore, one of ordinary skill in the art would have found it obvious to include a cache in between the processor and main memory of Potash in order to present a larger and faster address space to the processor (see Patterson p.541-2), as well as allowing the fetching of a fetch instruction from the main memory if it is not in the cache based on the control signal that indicates the need for a fetch (see Potash Col.7 lines 35-52 and Col.8 lines 6-12).

14. Regarding claim 2, Potash in view of Patterson has taught the memory data access structure according to claim 1 as shown above, wherein the control signal indicates whether the instruction executed in the current stage is a taken branch instruction (see Col.7 lines 35-52 and Col.8 lines 6-12).

15. Regarding claim 3, Potash in view of Patterson has taught the memory data access structure according to claim 1 as shown above, further comprising a program counter (38 of Fig.4) to store an address of the instruction currently executed among all the instructions to be executed (see Col.6 lines 53-64). Furthermore, it is well known in the art that the program counter holds the address of the current instruction being executed (see Patterson p.133).

16. Regarding claim 4, Potash in view of Patterson has taught the memory data access structure according to claim 3 as shown above, further comprising a multiplexer to receive the result signal output by the execution unit and the executed address stored in the program counter plus a set value, and to select one of the signals as the address signal (see Col.2 lines 35-46 and Col.8 lines 4-26). While not taught explicitly, it is inherent that a multiplexer selects, using the control signal (18 of Fig.1), between the branch target address and the sequential address. Here, the module "C" executes the instruction and determines whether the branch instruction will be taken or not (see Col.2 lines 35-39), which necessitates the need to arbitrate between the two addresses available so that only one address is supplied back to the "IPF" module for re-fetching. Furthermore, the "set value" that is added to the program counter is well known in the art. Because the program counter holds the address of the instruction being currently executed, and because Potash is fetching the next sequential address or the branch target address, then the next

sequential address is simply the current address plus an offset of a set amount, which will be determined by how the instructions are addressed in the particular architecture.

17. Regarding claim 5, Potash has taught a memory data access structure suitable for use in a processor, comprising:

a. A memory (M of Fig.1), to store and output an instruction according to an address signal (see Col.1 lines 16, 19-20 and Col.6 lines 33-36),

b. A pipeline processor (see Col.1 lines 10-18) for executing a plurality of processor instructions, including an execution unit ("EX" of Fig.1) to perform an execution operation on the instruction transferred from a previous stage (see Col.1 lines 30-37), and to output a result signal (see Col.1 lines 25-28, 47-48),

c. A branch instruction prediction mechanism (IPF of Fig.4), to output a predicted address according to a fetch instruction (see Col.4 lines 36-44, Col.5 lines 56-65, Col.6 lines 46-67, and Col.7 lines 1-5),

d. A comparator, to receive the result signal and the predicted address and to output a comparison signal (see Col.2 lines 35-46 and Col.8 lines 7-26), wherein:

i. When the execution unit is executing a branch instruction, the result signal is a target address, wherein the target address is selected to be an address signal output to the memory, wherein a next instruction to be executed is fetched according to the address signal (see Col.2 lines 35-46),

ii. When the execution unit is executing the branch instruction, the processor fetches the fetch instruction, and the result signal obtained after executing the branch instruction is transferred to the comparator, the comparator

then outputs the comparison signal to the memory according to the result signal and the predicted address (see Col.2 lines 35-46 and Col.8 lines 7-26).

18. Potash has not taught a cache memory configured between the main memory and the processor that receives an address signal, nor has Potash taught that if the fetch instruction is not store din the cache memory, the cache memory determines whether to fetch the fetch instruction from an external memory according to the comparison signal.

19. However, Patterson has taught the use of a memory hierarchy in modern microprocessors, consisting of multiple levels of memory of varying size and speed in order to create the appearance of a larger, faster memory space, while keeping costs minimized versus having a single large memory (see p.541-2). Furthermore, the general configuration of this hierarchy consists of a cache between the main memory and the processor (see p.545), which operates in a manner such that when a fetch of data at an address results in a cache miss, the data is instead brought from memory into the cache and processor (see p.545, 550). Therefore, one of ordinary skill in the art would have found it obvious to include a cache in between the processor and main memory of Potash in order to present a larger and faster address space to the processor (see Patterson p.541-2), as well as allowing the fetching of a fetch instruction from the main memory if it is not in the cache based on the control signal that indicates the need for a fetch (see Potash Col.7 lines 35-52 and Col.8 lines 6-12).

20. Regarding claim 6, Potash in view of Patterson has taught the memory data access structure according to claim 5 as shown above, wherein the comparison signal is generated after

performing comparison operation upon the result signal and the predicted address (see Col.2 lines 35-46 and Col.8 lines 7-26).

21. Regarding claim 7, Potash in view of Patterson has taught the memory data access structure according to claim 5 as shown above, further comprising a program counter (38 of Fig.4) to store an address of an instruction which is executed currently among all the instruction to be executed (see Col.6 lines 53-64). Furthermore, it is well known in the art that the program counter holds the address of the current instruction being executed (see Patterson p.133).

22. Regarding claim 8, Potash in view of Patterson has taught the memory data access structure according to claim 7, comprising further a multiplexer to receive the result signal output from the execution unit, an execution address stored in the program counter plus a signal with a determined value, and the predicted address, and to select one of these signals as an address signal (see Col.2 lines 35-46 and Col.8 lines 4-26). While not taught explicitly, it is inherent that a multiplexer selects, using the control signal (18 of Fig.1), between the branch target address and the sequential address. Here, the module "C" executes the instruction and determines whether the branch instruction will be taken or not (see Col.2 lines 35-39), which necessitates the need to arbitrate between the two addresses available so that only one address is supplied back to the "IPF" module for re-fetching. Furthermore, the "set value" that is added to the program counter is well known in the art. Because the program counter holds the address of the instruction being currently executed, and because Potash is fetching the next sequential address or the branch target address, then the next sequential address is simply the current address plus an offset of a set amount, which will be determined by how the instructions are addressed in the particular architecture.

23. Regarding claim 9, Potash has taught a method of memory data access suitable for use in a processor, comprising:

a. Providing an instruction according to an address signal (see Col.1 lines 16, 19-20 and Col.6 lines 33-36),

b. Executing the instruction to output a result signal and a control signal (see Col.1 lines 25-37, 47-48, Col.7 lines 35-52 and Col.8 lines 6-12),

c. Fetching a next instruction to be executed according to an address signal, wherein when the instruction is a branch instruction, the result signal is a target address, wherein the target address is selected to be the address signal output to the memory (see Col.2 lines 35-46),

24. Potash has not taught a cache memory configured between the main memory and the processor that receives an address signal, nor has Potash taught determining whether a fetch instruction is fetched from an external memory according to the control signal when the processor is fetching the fetch instruction and the fetch instruction is not stored in the cache memory.

25. However, Patterson has taught the use of a memory hierarchy in modern microprocessors, consisting of multiple levels of memory of varying size and speed in order to create the appearance of a larger, faster memory space, while keeping costs minimized versus having a single large memory (see p.541-2). Furthermore, the general configuration of this hierarchy consists of a cache between the main memory and the processor (see p.545), which operates in a manner such that when a fetch of data at an address results in a cache miss, the data is instead brought from memory into the cache and processor (see p.545, 550). Therefore, one of

ordinary skill in the art would have found it obvious to include a cache in between the processor and main memory of Potash in order to present a larger and faster address space to the processor (see Patterson p.541-2), as well as allowing the fetching of a fetch instruction from the main memory if it is not in the cache based on the control signal that indicates the need for a fetch (see Potash Col.7 lines 35-52 and Col.8 lines 6-12).

26. Regarding claim 10, Potash in view of Patterson has taught the method according to claim 9 as shown above, wherein the control indicates whether the instruction currently executed is a taken branch instruction (see Col.7 lines 35-52 and Col.8 lines 6-12).

27. Regarding claim 11, Potash in view of Patterson has taught the method according to claim 9 as shown above, comprising further the step of selectively outputting the result signal and an address of the instruction executed currently plus a signal with a certain value (see Col.2 lines 35-46 and Col.8 lines 4-26).

28. Regarding claim 12, Potash has taught a method for memory data access suitable for use in a processor, comprising:

a. Providing an instruction (see Col.1 lines 19-20),

b. Executing the instruction to output a result signal (see Col.1 lines 25-28, 30-37, 47-48),

c. Using a branch prediction mechanism to receive a fetch instruction and to output a predicted address (see Col.4 lines 36-44, Col.5 lines 56-65, and Col.6 lines 46-64),

d. Comparing the result signal with the predicted address, and outputting a comparison signal, wherein:

i. When the instruction being executed is a branch instruction, the result signal is a target address and is selected to be an address signal, and the processor fetches an instruction to be executed next according to the address signal (see Col.2 lines 35-46).

29. Potash has not explicitly taught that while executing the branch instruction, the processor fetches the fetch instruction, and if the fetch instruction is not in a cache memory, according to the comparison signal, the cache memory determines whether to fetch the fetch instruction from an external memory.

30. However, Patterson has taught the use of a memory hierarchy in modern microprocessors, consisting of multiple levels of memory of varying size and speed in order to create the appearance of a larger, faster memory space, while keeping costs minimized versus having a single large memory (see p.541-2). Furthermore, the general configuration of this hierarchy consists of a cache between the main memory and the processor (see p.545), which operates in a manner such that when a fetch of data at an address results in a cache miss, the data is instead brought from memory into the cache and processor (see p.545, 550). Therefore, one of ordinary skill in the art would have found it obvious to include a cache in between the processor and main memory of Potash in order to present a larger and faster address space to the processor (see Patterson p.541-2), as well as allowing the fetching of a fetch instruction from the main memory if it is not in the cache based on the control signal that indicates the need for a fetch (see Potash Col.7 lines 35-52 and Col.8 lines 6-12).

31. Regarding claim 13, Potash in view of Patterson has taught the method according to claim 12 as shown above, comprising further a step of selectively outputting one of the result

signals, an address that the processor is currently processing plus a certain value, and the predicted address (see Col.2 lines 35-46 and Col.8 lines 4-26).

32. Regarding claim 14, Potash in view of Patterson has taught the method according to claim 12 as shown above, wherein the comparison signal indicates whether the branch instruction predicted by the branch prediction mechanism is correct (see Col.8 lines 7-26).

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

34. Sakamura et al., U.S. Patent No. 5,606,675, has taught a method for invalidating an instruction prefetch based on confirmed branch prediction data.

35. Moyer, U.S. Patent No. 5,951,678, has taught a method for prefetching instructions based on branch prediction data.

36. Poplingher et al., U.S. Patent No. 6,185,676, has taught a pipelined microprocessor implementing branch prediction that updates the fetch path after execution of the branch instruction.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
11/19/2003

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